CLAIMS

I/We claim:

[c1] 1. A device for protecting a gate terminal and lead of a gate electrode line at stage of scribing and spalling a liquid crystal display panel, said liquid crystal display panel comprising a first substrate with thin film transistor array thereon and a second substrate thereon with color filter opposite to said thin film transistor array, said device comprising:

a resist region covering said gate terminal and said lead of the gate electrode line and between a passivation layer and a gate insulating layer, said resist region located at a scribing line on margin of the second substrate of the panel.

[c2] 2. The device according to claim 1, wherein material of said resist region is metal.

[c3] 3. The device according to claim 2, wherein said resist region is a floating region.

[c4] 4. The device according to claim 2, wherein material of said resist region is the same as source/drain electrodes of the thin film transistor.

[c5] 5. The device according to claim 4, wherein said resist region is formed by a step of said source/drain electrodes.

[c6] 6. The device according to claim 5, wherein said resist region is formed by steps comprising:

providing said array substrate with a gate electrode and said gate electrode line thereon, and said gate insulating layer covering said gate electrode, said gate electrode line, and said array substrate;

forming an island semiconductor layer on said gate insulating layer and over said gate electrode;

depositing a blanket metal layer on said island semiconductor layer and said gate insulating layer;

performing a lithographic process to said conductive layer by using a reticle with a source pattern and a drain pattern on said gate electrode and a resist region pattern on said gate terminal and said lead; and

etching said conductive layer to form said source/drain electrodes and said resist region.

[c7] 7. The device according to claim 1, wherein material of said resist region is the same as island semiconductor layer of the thin film transistor.

[c8] 8. The device according to claim 7, wherein said resist region is formed by a step of formation of said island semiconductor layer.

[c9] 9. The device according to claim 8, wherein said resist region is formed by steps comprising:

providing said array substrate with a gate electrode and said gate electrode line thereon, said gate insulating layer blanket on said gate electrode, said gate electrode line, and said array substrate;

depositing a blanket semiconductor layer on said gate insulating layer;

performing a lithographic process to said semiconductor layer by using a reticle with an island pattern on said gate electrode and a resist region pattern on said gate terminal and said lead; and

etching said semiconductor layer to form said island semiconductor layer and said resist region.

[c10] 10. The device according to claim 1, wherein activity of said resist region is less than said gate electrode line.

[c11] 11. The device according to claim 1, wherein distance between said scribing line and margin of said resist region is about more than 50 μm.

[c12] 12. The device according to claim 11, wherein width of said resist region is larger than said gate terminal and said gate electrode line.

[c13] 13. A method for protecting a gate terminal and lead at stage of scribing and spalling a liquid crystal panel, said method comprising:

providing a first substrate;

forming the gate electrode and the gate electrode line on said first substrate, wherein said gate electrode line comprises said gate terminal and said lead;

depositing a blanket gate insulating layer on said gate electrode, said gate electrode line, and said substrate;

forming an island semiconductor layer on said gate electrode and a source electrode and a drain electrode on said island semiconductor layer, and simultaneously forming a resist region on said gate insulating layer and covering said gate terminal and said lead of a gate electrode line, said resist region located at a scribing line on margin of a second substrate with color filter thereon;

depositing a blanket passivation layer on said source electrode, said drain electrode, and said resist region.

[c14] 14. The method according to claim 13, wherein said resist region is formed of metal.

[c15] 15. The method according to claim 14, wherein said resist region is floating.

[c16] 16. The method according to claim 15, wherein said step of formation said floating metal resist region is at a step of formation of said source electrode and said drain electrode.

[c17] 17. The method according to claim 16, wherein formation of said floating metal resist region comprises:

forming an island semiconductor layer on said gate insulating layer and over said gate electrode;

depositing a blanket metal layer on said island semiconductor layer and said gate insulating layer;

performing a lithographic process to said conductive layer by using a reticle with a source pattern and a drain pattern on said gate electrode and a resist region pattern on said gate terminal and said lead; and

etching said conductive layer to form said source electrode, said drain electrode and said floating metal resist region.

[c18] 18. The method according to claim 15, wherein activity of said floating metal resist region is less than said gate electrode line.

[c19] 19. The method according to claim 15, wherein distance between said scribing line and margin of said floating metal resist region is about more than 50 μm.

[c20] 20. The method according to claim 19, wherein width of said floating metal resist region is larger than said gate terminal and said gate electrode line.